UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/236,526	01/25/1999	FELIX KHOURI	081862.P119	1370

7590 08/12/2004

BLAKELY SOKOLOFF TAYLOR AND ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER	
TSEGAYE, SABA	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 08/12/2004

16

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/236,526	KHOURI ET AL.	
	Examiner	Art Unit	
	Saba Tsegaye	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9-14,16 and 18-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,9-14,16 and 18-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 18-27 and 60-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 18, 23 and 60 recite the limitation "said operating not" in line 4. There is insufficient antecedent basis for this limitation in the claims.

4. Regarding claims 18, 23 and 60, the phrase "discouraging the occurrence of an error" is vague. It is not clear what "discouraging" refers.

Claim Rejections - 35 USC § 103

5. Claims 1-5, 7, 9-14, 16, 28, 29, 31-34, 36-40, 42, 44-46, 48, 50, 51, 53, 55, 56, 58, 65, 66, 68 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Hess (4,751,670).

The Admitted prior art discloses a network switch having a processor card including a memory, a stats table (as in claims 4 and 13), and a routing table (as in claims 3 and 12) that contains the list of current connections (page 3). Further, the Admitted prior art discloses that when a non-recoverable (non-ignorable) software error occurs in the processor unit of the active processor card, the processor has to reset the switch by clearing the computer memory.

However, the Admitted prior art does not expressly disclose the following steps: determining if an error is ignorable; determining whether a threshold has been reached if the error is determined to be ignorable, the threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time; and performing a hitless rebuild in the processor card (as in claims 1, 9 and 10); setting the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached (as in claims 7 and 16) and protecting a portion of the memory from access by the processing unit during the initialization (as in claims 2-5 and 11-14).

Regarding claims 1, 9 and 10, Hess teaches, in Figs. 1 and 2, that a digital data processor detects disruptions (claimed detecting an error); and determining if the error is ignorable (column 10, lines 20-30). Further, Hess teaches that a restart counter 21 is tested to determine if it has attained the count N (claimed determining whether a threshold has been reached if the error is determined to be ignorable), N represents the number of processing resumption attempts and a nominal quantity for N would be approximately five unsuccessful restart attempts (claimed the threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time). If the count N has not been attained, program flow retunes to the initialization block (claimed performing a hitless rebuild in the processor card) (column 9, lines 11-46).

It would have been obvious to one ordinary skill in the art at the time the invention was made to use the teachings from Hess of adding a method of steps (that determining if the error is ignorable; whether a threshold has been reached if the error is determined to be ignorable; the

threshold corresponding to a number of hitless rebuilds that have occurred within an amount of time; and performing a hitless rebuild) to the processor card disclosed by Admitted Prior Art. one of ordinary skill in the art would have been motivated to do this because the above method of steps provide a system having soft error recovery capability (column 3, lines 18-30) and, further, to provide a method and apparatus that precludes the logical processor from entering a loop of error detection and recovery from which it cannot escape (column 9, lines 30-33).

Regarding claims 2-5 and 11-14, Hess teaches the method wherein the performing of hitless rebuild includes: performing an initialization of the memory (column 3, lines 50-55); and protecting a portion of the memory from access by the processing unit during the initialization (column 4, lines 7-13).

It would have been obvious to one ordinary skill in the art at the time the invention was made to use the teachings from Hess of adding a protected memory to the processor card disclosed by the Admitted Prior Art. One of ordinary skill in the art would have been motivated to do this because adding a protected memory allows the system to store data (such as routing table, stat table) and to protect the data from destruction or permanent scrambling (column 4, lines 7-13).

Regarding claims 7 and 16, Hess teaches the method further comprising setting the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached (column 9, lines 16-20).

It would have been obvious to one ordinary skill in the art at the time the invention was made add a method that sets the processing unit to enter into a degraded mode if the error is not ignorable and if the threshold has been reached, such as that suggested by Hess, in the method of the Admitted Prior Art in order. One of ordinary skill in the art would have been motivated to do this because entering into a degraded mode precludes the logical processor from entering a loop of error detection and recovery from which it cannot escape (column 9, lines 30-33).

Regarding claims 28, 33, 38, 44, 50, 55 and 65, the Admitted Prior Art discloses all the claim limitations as stated above. Further, The Admitted Prior Art discloses that the processor card stores information regarding the topology of the network (routing table) and the status information for all other switches (state table). However, the Admitted Prior art does not expressly disclose a protected memory region that stores information that can be used by the processor to execute the software and re-initializing not deleting routing table information and state table information.

Hess teaches, in Fig. 1, a protected memory region (Non-Volatile RAM 17), and a non-protected memory region (ROM 11) for storing the operative program for performing all of the functions required by the computer 10 in the application in which it is utilized. The protected memory region to store information that can be used by the processor to execute the re-initializable software after the software has been reinitialized (the past values of the control and logic state variables are stored; column 4, lines 54-56); the re-initializable software comprising instructions for re-initializing the software in response to an error (column 4, lines 18-34; column 5, line 36-column 6, line 19) (as in claims 28, 33, 38, 44, 50, 55 and 65); the card not

comprising: error preventive packaging, that surrounds the protected memory region (column 4, lines 39-53) but not the non protected memory region (column 4, lines 7-13) (as in claims 28, 33, 50, 55 and 65). Further, Hess teaches that when an upset is detected and the application program is vectored to the reinitialization and restart location 12, the index counter 19 is decremented so that the current past values of the control and logic state variables are retrieved and utilized in the reinitialization and restart procedure (claimed reinitializing not deleting the state table information from the memory because the instructions are written to be unable to invoke memory addresses for a segment of the memory where the routing table information resides so to make the segment of the memory inaccessible during the reinitializing) (as in claims 38, 44).

It would have been obvious to one ordinary skill in the art at the time of the invention was made to use the teachings from Hess of adding a protected memory to the processor card disclosed by the Admitted Prior Art. One of ordinary skill in the art would have been motivated to do this because adding a protected memory allows the system to store data (such as routing table, stat table) and to protect the data from destruction or permanent scrambling (column 4, lines 7-13) and to provide a system having soft error recovery capability.

Regarding claims 31, 32, 36, 37, 42, 48, 53, 58, 68 and 69, the Admitted Prior Art discloses all the claim limitations as stated above. Further, The Admitted Prior Art discloses that the processor card stores information regarding the topology of the network (routing table) and the status information for all other switches (state table). However, the Admitted Prior art does not expressly disclose the protected memory region further comprises a segment of random access memory.

Hess teaches, in Fig. 1, that an index counter 19 is utilized to index the reading and writing accesses to the RAM 17 by providing an offset that is added to the base address of the location in RAM 17 of a state variable to provide for **the multiple storage** thereof (column 4, lines 56-67).

It would have been obvious to one ordinary skill in the art at the time of the invention was made to add a segment of random access memory, such as that suggested by Hess, in the memory of the Admitted Prior Art in order to provide a memory that data immune from compromise due to upset (column 3, lines 19-22).

Regarding claims **29, 34, 39, 40, 45, 46, 51, 56 and 66,** the Admitted Prior Art discloses all the claim limitations as stated above. Further, The Admitted Prior Art discloses that the processor card stores information regarding the topology of the network (routing table) and the status information for all other switches (state table). However, the Admitted Prior art does not expressly disclose a non-volatile memory.

Hess teaches, in Fig. 1, a non-volatile memory (RAM 17).

It would have been obvious to one ordinary skill in the art at the time of the invention was made to add non-volatile memory, such as that suggested by Hess, in the memory of the Admitted Prior Art in order to provide a memory that does not change state when the computer is reset and does not lose data when power is remove from it.

6. Claims **30, 35, 41, 46, 47, 52, 57 and 67** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Hess as applied to claims 18, 23, 28, 33, 38, 44, 50, and 55 above, and further in view of Rakavy et al. (US 6,324,644).

The Admitted Prior art in view of Hess discloses all the claim limitations as stated above. Further, Hess teaches in Fig. 1 a non-volatile memory RAM 17 and ROM 11.

However, the Admitted Prior art in view of Hess does not expressly disclose volatile memory.

Rakavy teaches, in Fig. 2, a volatile memory and random access memory 120.

It would have been obvious to one ordinary skill in the art at the time of the invention was made to substitute a volatile memory, such as that suggested by Rakavy, to the memory of the Admitted prior art in view of Hess in order to provide a memory that shared by another program or by an interrupt service routine.

7. Claims **43, 49, 54 and 59** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted prior art in view of Hess as applied to claims 18, 23, 28, 33, 38, 44, 50, and 55 above, and further in view of Treu (US 5,245,615).

The Admitted prior art in view of Hess discloses all the claim limitation as stated above except for dynamic random access memory.

Note that dynamic random access memories are more commonly used than RAMs because dynamic random memory is less expensive than static RAM and their circuitry is simpler.

True teaches that random access memory comprises dynamic random access memory (column 2, lines 65-67).

It would have been obvious to one ordinary skill in the art at the time the invention was made to use dynamic RAM, such as that suggested by True, in the memory of the Admitted prior art in view of Hess in order to provide less expensive memory.

Response to Arguments

8. Applicant's arguments with respect to claims 1-5, 7, 9-14, 16 and 18-69 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (703) 308-4754. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ST
July 30, 2004

JOHN PEZZLO
PRIMARY EXAMINER